

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DKT. NO. 501.43228X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT MURATA, et al.			
		FILING DATE January 14, 2004		GROUP	

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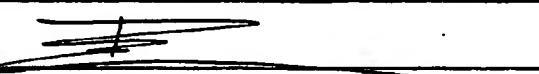
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
TL AA	5,198,683	03/30/1993	SIVAN	357	67	03/03/1993
TL AB	5,670,803	09/23/1997	BEILSTEIN, Jr. et al.	257	278	02/08/1995
TL AC	5,994,735	11/30/1999	MAEDA, et al.	257	329	11/30/1999
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TL AM	11-176936	07/02/1999	JP	HO1L	21/768	X	
TL AN	9-232447	09/05/1997	JP	HO1L	21/8244	X	
TL AO	2001-28443	01/30/2001	JP	HO1L	29/786	X	
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TL AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
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		07/05/05